REMARKS/ARGUMENTS

Claims 2-14 and 16-20 remain pending in the application.

Claims 2-14 are rejected under 35 U.S.C. §103 as being unpatentable over *Rates* (US 5,677,203) in view of *Camilletti et al* (US 6,451,681 hereinafter *Camilletti*).

Claims 16-20 are rejected under 35 U.S.C. §103 as being unpatentable over *Weiler* (US 5,559,056) in view of *Camilletti*.

The Cited References

Rates "relates to the testing and burn-in of semiconductor devices for use in complex integrated circuits. In particular, the invention relates to a modified tape automated bonding process for providing known good bare die (col. 1, lines 15-18). Furthermore, *Rates* provides "A process for providing a temporary, non-intrusive electrical connection to bond pads of a semiconductor die permitting test and burn-in of bare die. Modified tape automated bonding (TAB) techniques are used with gold bumped die bond pads for providing known good die (KGD). After test and burn-in, the temporary connection to the die is removed without the need to reform the gold bumps prior to use in a multichip module. Gold inner leads of a TAB tape are diffusion bonded to gold bumps wherein the bonding is sufficient for providing electrical connection during the testing and burn-in of the die yet sufficiently weak for removal of the leads from the die after testing and burn-in. The process provides the KGD necessary for acceptable first assembly yields and long term reliability of multichip modules (MCM). Bare die with gold bumped, sealed bond pads are provided simplifying interconnection during testing and ultimate module use (Abstract).

Weiler "relates generally to bond pads fabricated on a semiconductor die. More specifically, during formation of a bond pad, a barrier layer is deposited over the metallization layer, the barrier layer is masked, and subsequently both the barrier layer and the metallization layer are etched in one step. Thereafter a

bonding layer is formed over the barrier layer, preferably using an electrolysis process (col. 1, lines 5-12)." Furthermore, *Weiler* provides, "a method for fabricating bond pads on a semiconductor device that reduces intermetallic growth between a metallization layer and a bonding layer is discussed. Initially a metallization layer is deposited over a substrate. Following steps include depositing a barrier layer over the metallization layer, masking a portion of the barrier layer, and etching the barrier layer and the metallization layer. Etching of the barrier and masking layers is performed utilizing the barrier layer mask as a mask for both the barrier layer and the metallization layer. Further steps include depositing a non-conductive layer conformally overlying the barrier layer, masking a portion of the non-conductive layer, and etching the non-conductive layer. Etching the non-conductive layer forms an exposed region of the barrier layer. A later step of this method includes forming a bond layer over the exposed region of the barrier layer, with one possible formation method utilizing an electrolysis process. Thus a bond pad with a capped metallization layer is produced with only two mask and etch steps. This bond pad will withstand ambient temperatures up to approximately 200.degree. C. (Abstract).

Camilletti et al. is directed to a semiconductor integrated circuit chip or die more suitable in testing as an unpackaged die. A semiconductor integrated circuit (IC) die is made with enhanced resilience to handling, testing, and storage, associated with its qualification and distribution as a KNOWN GOOD DIE (KGD). The IC device has a mechanically tough and chemically inert top layer to protect it from damage. The device contacts are made of thin film metals which facilitate reversible electrical connections used in KGD testing. The overall contact structure protects the device from irreversible damage during the connection, test, and disconnection sequence.

Applicants Invention

In contrast with the cited references, Applicants' invention is directed to semiconductor devices and their fabrication particularly, their manufacture

involving techniques for forming circuitry. One aspect of semiconductor manufacture includes the formation of bond pads on a chip. The bond pads are normally placed on the periphery of the semiconductor chip, without underlying circuitry, and are used for subsequent wire bonding to a wafer. However, it is desirable to form bond pads over active circuitry in order to reduce the size of the chip.

In an example embodiment of the present invention, a metal bond pad is formed on a semiconductor chip. The metal bond pad has a first metal pad layer, a TiN diffusion layer over the first metal pad layer, and a second metal pad layer over the TiN diffusion layer. A passivation layer is formed over the pad and subsequently etched to expose the second metal pad layer

In another example embodiment of the present invention, a system is arranged for manufacturing a semiconductor chip having a metal bond pad over active circuitry. A first metal deposition arrangement is adapted to deposit a metal bond pad on the circuit side, and a second metal deposition arrangement is adapted to deposit a metal layer over the circuit side. After the metal layer is deposited, a photoresist deposition arrangement is adapted to pattern a photoresist mask over the metal layer, and an etching arrangement is adapted to etch the circuit side and remove the portion of the metal layer not masked with the photoresist. When the circuit side has been etched, a photoresist removal arrangement is adapted to remove the photoresist.

The §103 Rejections

Claims 2-14

With respect to claims 2-14, Applicants respectfully traverse the §103 rejections raised in the present Office Action.

The Office Action (page 3, lines 1-2) concedes that *Rakes* does not teach the feature of TiN of Applicants' invention. Applicants' claimed invention addresses a long-felt need to reduce the size of a device chip by placing wire

bonding areas over active circuits in the device chip. As mentioned earlier, unlike Applicants' invention, *Rates* is directed toward providing a temporary, non-intrusive electrical connection to bond pads of a semiconductor die permitting test and burn-in of bare die. *Rates* is *not* concerned with the formation of bond pads over active device area and thus does not teach or suggest Applicants' invention.

MPEP §2143.01 provides:

> **The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior are also suggests the desirability of the combination.** *In re Mills, 916 F.2d 680, 16USPQ2d 1430 (Fed. Cir 1990)*

In addition, *Rates* does not suggest or teach using TiN, consequently there would be no motivation to combine *Rates* with *Camilletti*. Although *Camilletti* describes the use of TiW or TiN for a diffusion barrier layer, one skilled in the art necessarily could not merely substitute "TiN" instead of "TiW" for a diffusion barrier layer, as it relates to *Rates* simply because one material versus another is "merely a preference. *Rates* employs his own particular process. To modify *Rates*' TiW process with TiN, would destroy the intent of *Rates*. Therefore, the two references are not properly combinable.

Furthermore, *Rates* does not claim the feature of "the metal bond pad and the metal layer include the same type of metal." In reviewing *Camilletti et al.* (col. 8, lines 8-14) as cited in the Office Action, the "same metal" layers are bumps of gold or solder. For example, "Layer 16A is most preferably a gold or solder (95PB-5Sn) bump, although it can be any metal which is stable in the environment. . ." The unlike the "metal bond pad and the metal layer" as taught by Applicants' invention. Combining these two references does not teach or suggest Applicants' claim. Modifying Camilletti et al. with Rates destroys the intent and purpose of Camilletti et al. See *In Re Gordon, 7333 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)*

In the absence of discussion on thickness of the TiN layer, the assertion that only routine experimentation is required to determine the thickness of the diffusion barrier of Applicants' invention is not a sufficient basis in making a case

of obviousness under §103. *In re Evanaega*, 829 F.2d 1110, 4 USPQ2d 1249 (Fed. Cir. 1987), there was no showing of *prima facie* obviousness in that:

> **The mere absence [from the reference] of an explicit requirement [of the claim] cannot be reasonably construed as an affirmative statement that [the requirement is in the reference.**

With respect to the diffusion barrier (claim 13) is constructed and arranged to mitigate inter-metallic Al/Au compounds. *Rates* cites use of "first field metals layer 20 of titanium and tungsten (TiW) is vacuum deposited. . .(col. 5, lines 34-35)." Consequently, *Rates* does not teach or suggest the use of TiN with respect to mitigation of inter-metallic compounds.

In that the case for a §103 rejection has not been made, claims 2-14, as presented, are allowable.

Claims 16-20

With respect to claims 16-20, Applicants respectfully traverse the §103 rejections raised in the present Office Action.

The Office Action concedes that *Weiler* does not teach the feature of TiN in Applicants' invention as discussed *supra*. *Camilletti* in that is directed to a semiconductor integrated circuit chip or die more suitable in testing as an unpackaged die, does not teach or suggest Applicants' claimed invention. Also, the technologies outlined in each reference would not necessarily be compatible with one another. Modifying either reference in making the combination would destroy the intent of each reference. The CCPA and the Federal Circuit have consistently held that when a §103 rejection is based upon a modification of a reference that destroys the intent, purpose or function of the invention disclosed in the reference, such a proposed modification is not proper and a *prima facie* case

of obviousness can not be properly made. See *In Re Gordon, 7333 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)*

In that claim 16, as presented, is allowable over the cited references, those claims depending therefrom are also allowable. Consequently, claims 17-20 are allowable.

Conclusion

In light of the amendments and arguments presented, Applicants believe they have addressed the Examiner's concerns. Therefore, the claims are allowable. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Please charge any fees other than the issue fee and credit any overpayments to Deposit Account 14-1270.

Respectfully submitted,

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By Peter Zawilski
Peter Zawilski
Registration No. 43,305
(408) 474-9063

Correspondence Address:

Intellectual Property & Standards
Philips Electronics North America Corporation
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131 USA

CUSTOMER NUMBER: 24738